IN THE UNITED STATES DISTRICT COURT FOR THE MIDDLE DISTRICT OF NORTH CAROLINA

THE TRUSTEES OF PURDUE UNIVERSITY, Plaintiff, vs. WOLFSPEED, INC. Defendant.	Civil Action No: 1:21-cv-840 **Jury Trial Demanded**

DEFENDANTS' OPENING CLAIM CONSTRUCTION BRIEF

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I. INTRODUCTION

Pursuant to LR 104.5 and the parties' Amended Rule 26(f) Report (Dkt. 73-1), Defendant Wolfspeed Inc. ("Wolfspeed") submits its opening brief concerning claim construction for disputed terms in claims 9 and 10 (the "Asserted Claims") of U.S. Patent No. 7,498,633 (the "'633 Patent").

II. TECHNOLOGY OVERVIEW[1]

The '633 Patent is directed to "semiconductor devices for high-voltage power applications," and specifically "metal-oxide semiconductor field-effect transistors" ("MOSFETs") formed from a material called silicon carbide ("SiC"). '633 Patent at 1:10-21, 1:44-45. A MOSFET is an electronic device used to regulate current in a variety of applications, such as computers, mobile phones, and automobiles. Ex. ¶ 1. A frequent application is battery-charging circuits, in which MOSFETs are used to switch current on and off to ensure the battery does not overcharge or overheat. *Id.*

The image below depicts a cross-section of a prior-art MOSFET developed by Wolfspeed. *See* Ex. 5 at Fig. 2A.[2] The device includes the following elements: a substrate (blue); drift layer (tan); JFET region and JFET limiting layer (pink); base regions (cyan);

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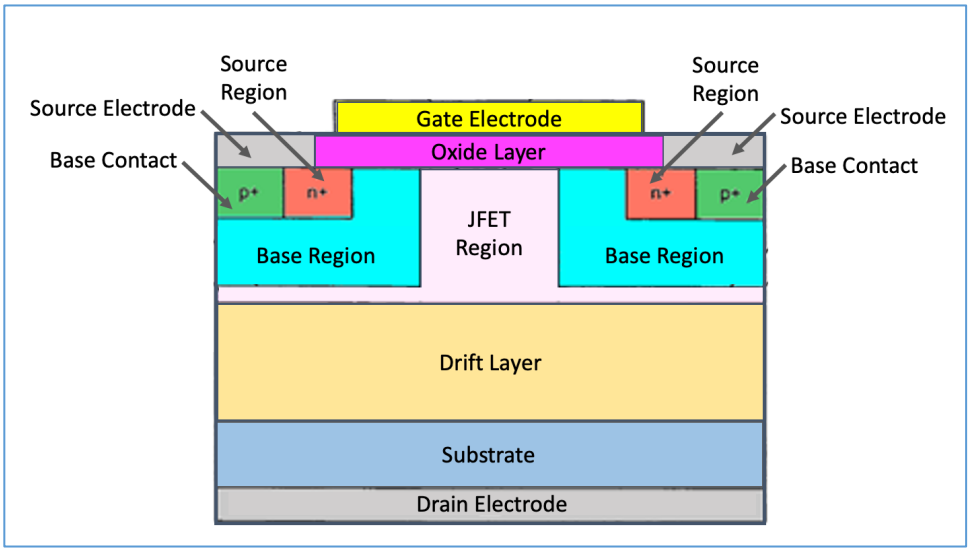
[1] Wolfspeed's opening brief is accompanied by the declaration of Dr. Alan Doolittle, who currently serves as the Joseph M. Pettit Professor in the School of Electrical and Computer Engineering at Georgia Institute of Technology. Ex. 1 ¶¶ 7-25. Dr. Doolittle and has nearly three decades of experience working with semiconductor devices, including silicon-carbide MOSFETs. *Id*. His declaration provides an overview of the technology at issue, along with opinions regarding indefiniteness.

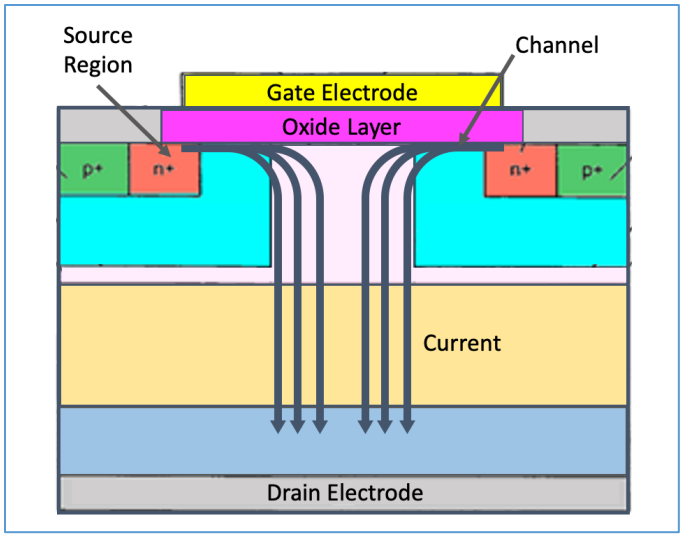
[2] Wolfspeed was formerly known as Cree, Inc. ("Cree").

source regions (red); base contact regions (green); source electrodes (gray); drain electrode (gray); gate electrode (yellow); and oxide layer (fuchsia):



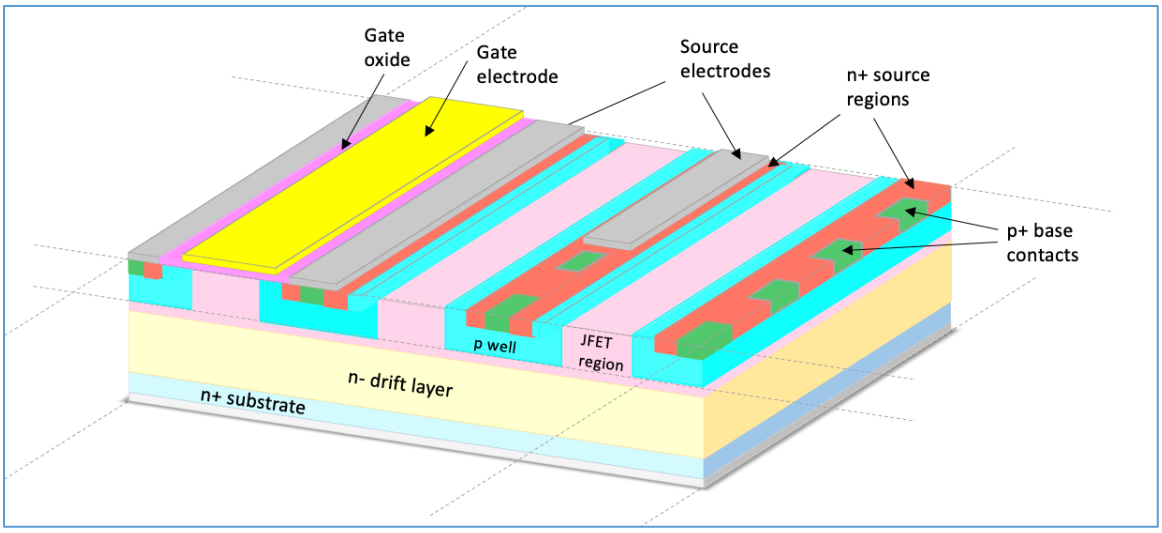
Id. (annotated).

The device depicted above is known as an *n* channel MOSFET, which means the substrate (blue), drift layer (tan), JFET region (pink) and source region (red) are doped with donor impurities ("*n* type"), while the base region (cyan) and base contact regions (green) are doped with acceptor impurities ("*p* type"). *See* Ex. 1 ¶¶ 32-34. Doping the semiconductor layers in this way allows current to flow between the source and drain electrodes when a voltage is applied to the gate. *Id.* ¶ 34. When the gate voltage is *positive*—referred to as the *on-state*—an electric field forms in the oxide layer, which attracts electrons and creates a channel under the gate. *Id.* The channel allows electrons to flow from the source regions (red) laterally and then downward through the drift layer (tan) to the drain as depicted:



Id.; Ex. 5 at Fig. 2A (annotated).

When the gate voltage is *negative*—referred to as the *off-state*—the electric field in the oxide layer repels electrons and prevents a channel from forming. Ex. 1 ¶ 34. Thus, current is blocked from flowing between the source and drain. *Id.* The images above show a cross-sectional view of a single MOSFET device and are often referred to as a "unit cell." In a real-world device, there are multiple parallel cells fabricated on a common substrate. This is illustrated in the image below, which provides a three-dimensional view of multiple cells:

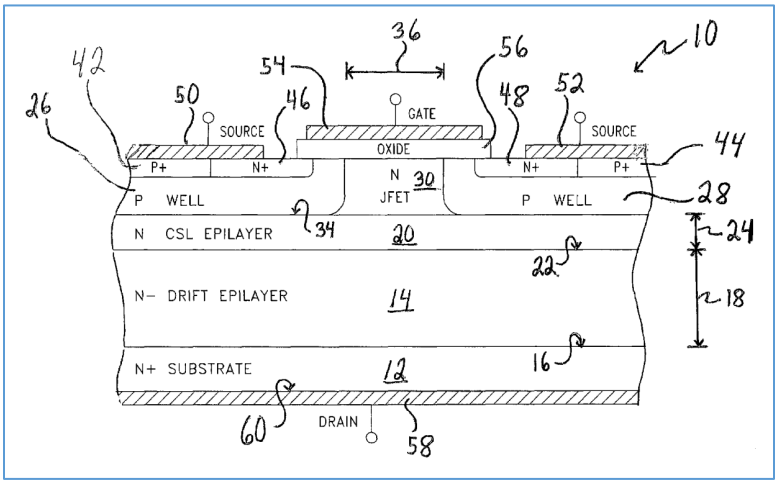


Early MOSFETs were designed primarily in silicon ("Si"), which was a widely available semiconductor material in the 1970s and 1980s. Ex. 1 ¶ 33. In the 1990s, researchers and industry participants began to explore silicon carbide ("SiC") as an alternative to silicon. *Id.* The SiC devices were seen as a promising alternative because they could withstand high voltages and temperatures, which made them well-suited for power applications. *Id.* ¶¶ 33, 40. SiC presented certain challenges in terms of processing technology and the availability of high-quality substrates. *Id.* It was apparent, however, that basic MOSFET structures used in silicon devices were readily applicable to SiC. *Id.* ¶¶ 40-41.

III. THE '633 PATENT

A. Specification

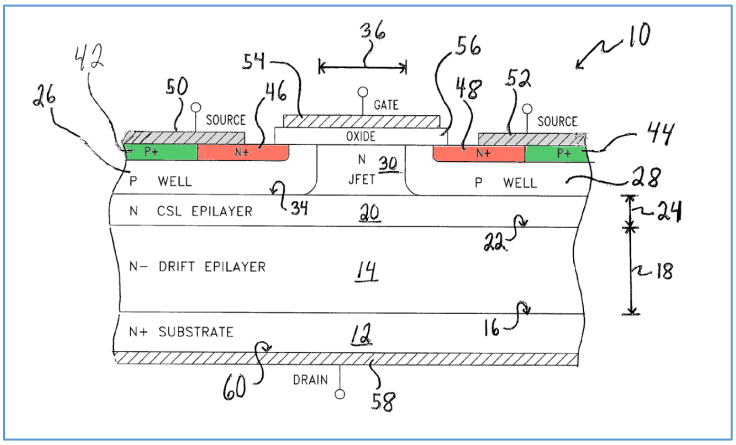
The '633 Patent is directed to MOSFETs for high-power applications. *See* '633 Patent at 1:18-36. Figure 1 illustrates the MOSFET device, which includes the same basic vertical structure and layers as was known in the prior art:



Id., Fig. 1.

The device 10 includes a SiC substrate 12 with successive semiconductor layers formed on the substrate. *Id*. at 4:4-6. On the front side 16 of the substrate 12 is a drift layer 14. *Id*. at 4:21-22. On the front side 22 of drift layer 14 is a current spreading layer 20 ("CSL"). *Id*. at 5:1-3. On the front side 34 of the CSL are first and second base regions 26, 28, with a JFET region 30 defined between them. *Id*. at 5:23-26. In some embodiments, the JFET region 30 has a width of less than about three microns, or alternatively about one micron. *Id*. at 6:24-27. Defined in the first and second base regions 26, 28 are first and second source regions 46, 48. *Id*. at 6:63-66. And defined in the first and second source regions 46, 48 are first and second base contact regions 42, 44. *Id*. at 6:66-67. And finally, first and second source electrodes 50, 52 are formed over the first and second source regions 46, 48. *Id*. at 7:4-6.

The '633 Patent describes different layouts for the source region of the MOSFET device. In the embodiment of Figure 3—which shows an overhead view of the device—the first and second base contact regions 158, 160 (which correspond to elements 42, 44 in Fig. 1) are spaced apart islands defined in the first and second source regions 154, 156 (which correspond to elements 46, 48 in Fig. 1). *Id*. at 7:57-63.



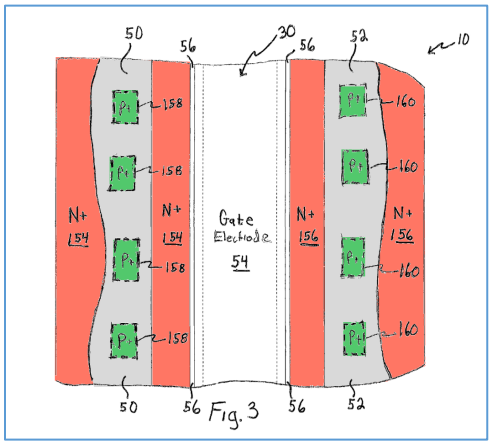


Fig. 3

Id. at Figs. 1, 3.

B. Asserted Claims

Purdue asserts claims 9 and 10 of the '633 Patent against Wolfspeed. Those claims are set forth below with disputed terms emphasized:

> 9. A double-implanted metal-oxide semiconductor field-effect transistor comprising:
>
> a silicon-carbide substrate;
>
> a drift semiconductor layer formed on a front side of the semiconductor substrate;
>
> a first source region;
>
> ***a first source electrode formed over the first source region***, the first source electrode defining a longitudinal axis;
>
> a plurality of first base contact regions defined in the first source region, each of the plurality of first base contact regions being spaced apart from each other in a direction parallel to the longitudinal axis defined by the first source electrode;
>
> a second source region;
>
> ***a second source electrode formed over the second source region***, the second source electrode defining a longitudinal axis;
>
> ***a plurality of second base contact regions defined in the second source region***, each of the plurality of second base contact regions being spaced apart from each other in a direction parallel to the longitudinal axis defined by the second source electrode; and
>
> ***a JFET region defined between the first source region and the second source region***, ***the JFET region having a width less than about three micrometers***.
>
> * * *

10. The double-implanted metal-oxide semiconductor field-effect transistor of claim 9, wherein ***the JFET region has a width of about one micrometer***.

C. Level of Ordinary Skill in the Art

A person of ordinary skill in the art ("POSITA") as of the effective filing date of the '633 Patent would have had an undergraduate degree in electrical engineering or an equivalent field, as well as 2-3 years of work experience in MOSFET design, with knowledge of different semiconductor materials, including SiC. Ex. 1 ¶ 50. Additional education reduces the threshold for years of experience in the field, and vice versa. *Id.*

IV. LEGAL STANDARD

A. Claim Construction

The words of a patent claim are generally given their "ordinary and customary meaning," which is "the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention." *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005). The "ordinary and customary meaning" is determined in the "context of the entire patent," including the specification and prosecution history. *Id*. The specification is "always highly relevant" to determine the meaning of a disputed term. *Id*. at 1315. The prosecution history will "often inform the meaning of the claim language by demonstrating how the inventor understood the invention and whether the inventor limited the invention in the course of prosecution, making the claim scope narrower than it otherwise would be." *Id*. at 1317. Extrinsic evidence—such as dictionaries, treatises, and expert testimony—may also "assist the court in determining the meaning of particular terminology to those of skill in the art of the invention." *Id*. at 1318. Extrinsic evidence

should not, however, be used to "contradict the meaning otherwise apparent from the intrinsic record." *Helmsderfer v. Bobrick Washroom Equip., Inc.*, 527 F.3d 1379, 1382 (Fed. Cir. 2008).

B. Indefiniteness

Patent claims are subject to a "definiteness" requirement, which means they must "particularly point[] out and distinctly claim[] the subject matter which the applicant regards as his invention." 35 U.S.C. § 112, ¶ 2. To satisfy the definiteness requirement, a patent claim must "inform those skilled in the art about the scope of the invention with reasonable certainty." *Nautilus, Inc. v. Biosig Instruments, Inc.*, 572 U.S. 898, 910 (2014). "A patent must be precise enough to afford clear notice of what is claimed, thereby apprising the public of what is still open to them." *Id*. at 909 (cleaned up). "Otherwise there would be a zone of uncertainty which enterprise and experimentation may enter only at the risk of infringement claims." *Id*. (cleaned up).

Following *Nautilus*, the Federal Circuit has explained that the "claims, when read in light of the specification and the prosecution history, must provide objective boundaries for those of skill in the art." *Interval Licensing LLC v. AOL, Inc.*, 766 F.3d 1364, 1371 (Fed. Cir. 2014). The Federal Circuit has found objective boundaries lacking—and the claims indefinite—when the claims recite a "term of degree" but the specification "fails to provide sufficient notice of its scope." *Id*. Objective boundaries are also lacking when the claims require a particular measurement, but the patent fails to explain how the measurement should be taken. *See Teva Pharms. USA, Inc. v. Sandoz, Inc.*, 789 F.3d 1335, 1341-42 (Fed. Cir. 2015) ("molecular weight" was indefinite because it could be measured

using different techniques, with potentially conflicting results, and the patent failed to provide guidance as to which technique should be used); *Dow Chem. Co. v. Nova Chems. Corp. (Can.)*, 803 F.3d 620, 630 (Fed. Cir. 2015) ("slope" was indefinite because the patent failed to explain how it should be measured).

V. DISPUTED TERMS

A. "a first source electrode formed over the first source region" and "a second source electrode formed over the second source region" (claim 9)

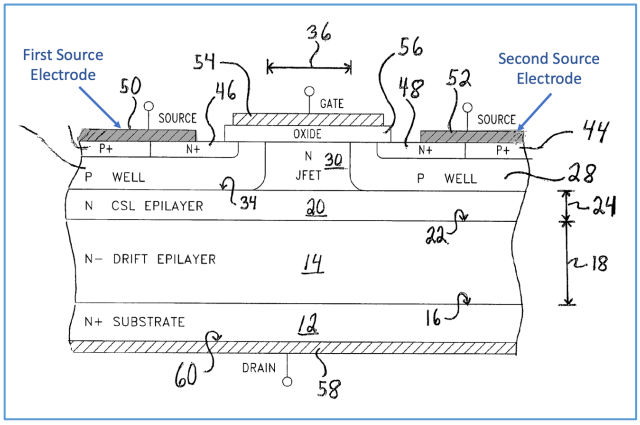
Wolfspeed's Proposal	Purdue's Proposal
The terms "first" and "second" require distinct elements (i.e., the "first source electrode" must be distinct from the "second source electrode")	No construction necessary.

Asserted claim 9 of the '633 Patent requires "a first source electrode formed over the first source region" and a "second source electrode formed over the second source region." The parties dispute whether the terms "first" and "second" require two distinct electrodes (as reflected in Wolfspeed's construction), or whether a single electrode could serve as both the "first" and "second" source electrodes (as Purdue appears to contend). The intrinsic record of the '633 Patent supports Wolfspeed's construction.

First, the claim language demonstrates that distinct electrodes are required. It uses the terms "first" and "second" as qualifiers for the "source electrode" terms, which "is a common patent-law convention to distinguish between repeated instances of an element or limitation." *3M Innovative Props. Co. v. Avery Dennison Corp.*, 350 F.3d 1365, 1371 (Fed. Cir. 2003). In *3M*, the terms "first" and "second" were used to connote distinct "patterns" in a method for embossing a film. *Id*. The same result was found in *Gillette Co. v. Energizer*

Holdings, Inc., where the terms "first, second, and third" were held to "distinguish different elements of the claim." 405 F.3d 1367, 1373 (Fed. Cir. 2005). Here, claim 9 uses the terms "first" and "second" to define distinct source electrodes, formed over different parts of the claimed MOSFET. *See* '633 Patent, claim 9. By contrast, nothing in the claim language suggests the "first" and "second" source electrodes may comprise a single electrode.

Second, the specification confirms that the "first source electrode" and "second source electrode" are distinct elements. The figures of the '633 Patent consistently illustrate the electrodes as separate and distinct, using different numerals 50 and 52 to identify each element:



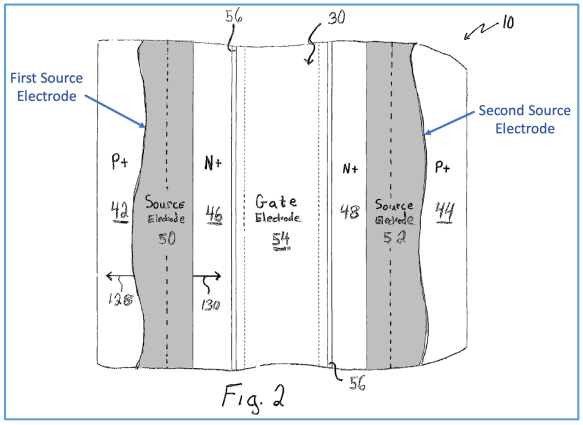


Fig. 2

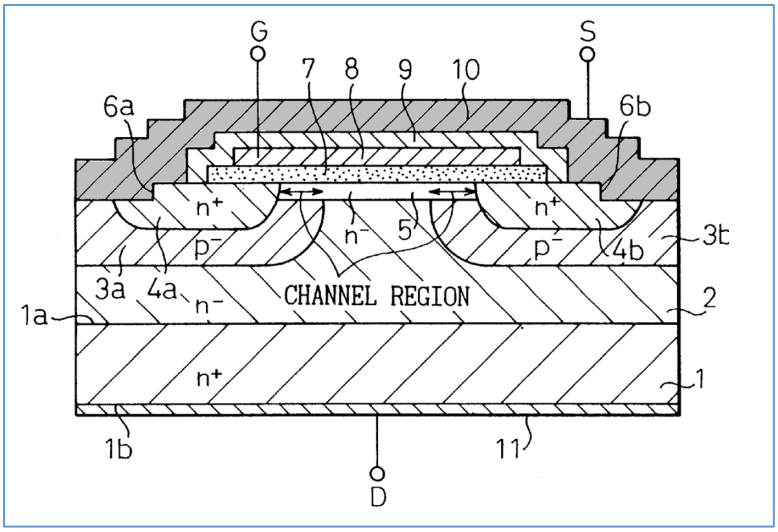
Id., Figs. 1, 2 (annotated).

Referring to these figures, the specification explains that "portions of the source regions 46, 48 and the base contact regions 42, 44 lie under the source electrodes 50, 52, ***respectively***," confirming that the source electrodes are distinct elements rather than a single structure. *Id.* at 7:27-33 (emphasis added), 8:14-16. The specification also describes misalignment of the source electrodes ***individually***—or relative to each ***respective*** source

region—which again confirms the electrodes are treated as distinct elements. *Id*. at 7:44-51.

Only once does the specification suggest that in "some embodiments, the source electrodes 50, 52 are coupled together to form a unitary source electrode." *Id*. at 7:6-7. The language of claim 9, however, distinguishes those embodiments by using the qualifiers "first" and "second" to indicate distinct, non-unitary, elements. *Id*. at claim 9; *3M*, 350 F.3d at 1371; *see also TIP Sys., LLC v. Phillips & Brooks/Gladwin, Inc.*, 529 F.3d 1364, 1373 (Fed. Cir. 2008) ("claims of the patent need not encompass all disclosed embodiments").

Third, the prosecution history of the '633 Patent further confirms that claim 9 was drafted to require distinct source electrodes rather than a single unitary structure. The principal dispute during prosecution was whether it would have been obvious to incorporate design features that were well known in Si-based MOSFETS into a SiC MOSFET as claimed. *See*, *e.g.*, Ex. 3 at 19-20 (October 12, 2007 Final Rejection at 3-4). To demonstrate that SiC devices were known in the prior art, the Examiner relied on U.S. Patent No. 6,573,534 ("Kumar"), which teaches a SiC MOSFET for high-power applications. *Id*. While Kumar teaches the same basic semiconductor layers as claim 9 of the '633 Patent, it uses a unitary source electrode 10 (shown in gray) to cover the entire top surface of the device:



Ex. 8 at Fig. 1 (annotated).

To overcome the Examiner's reliance on Kumar, Purdue amended claim 9 (which was pending as claim 12 during prosecution) to require distinct "first source electrode" and "second source electrode." Ex. 3 at 42 (March 12, 2008 Amendments at 4). The amended claim is reproduced below, with newly added limitations shown in underline:

12. (Currently Amended) A double-implanted metal-oxide semiconductor field-effect transistor comprising:

a ~~silicone carbide~~ silicon-carbide substrate;

a drift semiconductor layer formed on a front side of the semiconductor substrate;

a first source region;

a first source electrode formed over the first source region, the first source electrode defining a longitudinal axis;

a plurality of first base contact regions defined in the first source region, each of the plurality of first base contact regions being spaced apart from each other in a direction parallel to the longitudinal axis defined by the first source electrode;

a second source region;

a second source electrode formed over the second source region, the second source electrode defining a longitudinal axis;

a plurality of second base contact regions defined in the second source region, each of the plurality of second base contact regions being spaced apart from each other in a direction parallel to the longitudinal axis defined by the second source electrode; and

a JFET region defined between the first source region and the second source region, the JFET region having a width less than about three micrometers.

Id.

By amending claim 9 to distinguish the unitary source electrode of Kumar, Purdue limited the claimed MOSFET to embodiments that require distinct "first" and "second" source electrodes. *SIMO Holdings, Inc. v. Hong Kong uCloudlink Network Tech. Ltd.*, 983 F.3d 1367, 1379 (Fed. Cir. 2021) ("the language of the claim itself makes clear that …claim 8 does not cover specification embodiments that lack a non-local calls database.").

Accordingly, the claims, specification, and prosecution history support Wolfspeed's proposed construction, which requires the "first" and "second" source electrodes to be distinct elements.

B. "a JFET region defined between the first source region and the second source region, the JFET region having a width" (claim 9)

Wolfspeed's Proposal	Purdue's Proposal
Indefinite	No construction necessary.

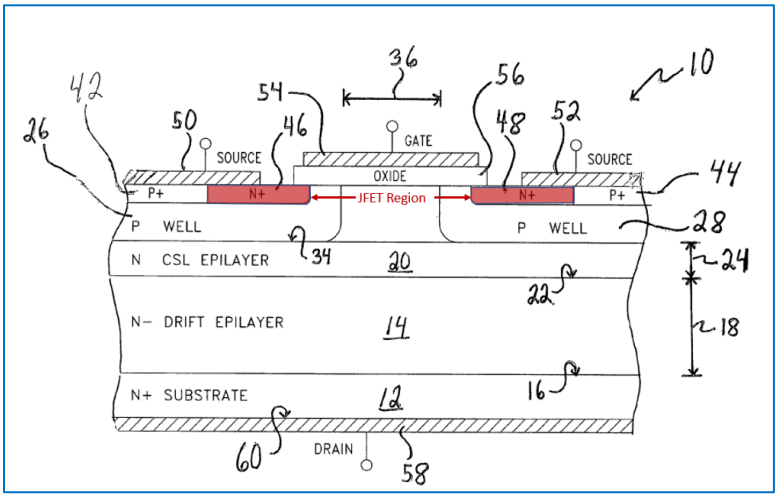
Claim 9 of the '633 Patent requires "a JFET region defined between the first source region and the second source region." '633 Patent, claim 9. In the context of the Asserted Claims, the JFET region must satisfy certain width requirements. Claim 9 requires a width of "less than about three micrometers," and claim 10 requires a width of "about one micrometer." *Id*., claims 9-10.[3] Because the JFET region serves as the basis for determining whether those requirements are satisfied, there must be reasonable certainty about how and

[3] Micrometers are a unit of length equal to 0.001 millimeter. Micrometers are referred to in the art as *microns* and designated with the symbol μm.

where to measure its width. The '633 Patent fails to provide reasonable certainty—and thus renders the asserted claims indefinite—for the following reasons.

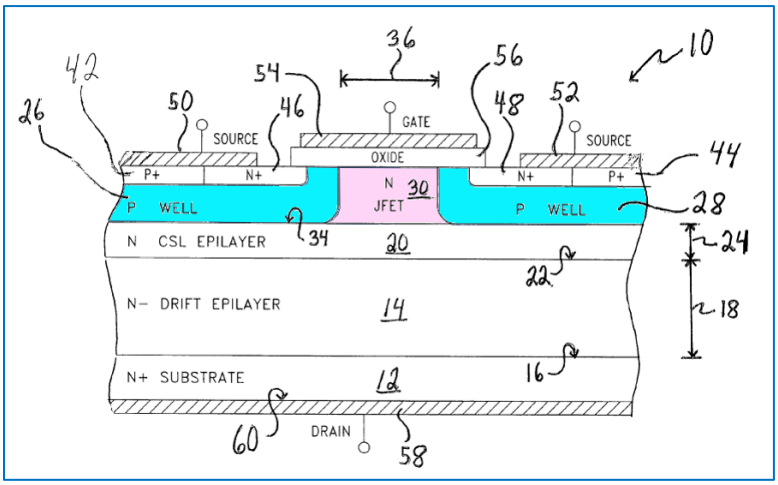
1. The Claim Language Conflicts With the Specification

Claim 9 expressly requires the JFET region to be "defined between the first source region and the second source region." In the context of patent claiming, the term "defined between" sets forth the boundaries or extent of the element being "defined." *See WIMCO, LLC v. Lange Indus., Inc.*, No. 06-CV-3565, 2007 WL 4461629, at *12 (D. Minn. Dec. 14, 2007) ("To define an opening, however, is to establish its boundaries.") (quotation omitted). That is consistent with the ordinary and customary meaning of "define," which is "to delineate the outline or form of." Ex. 10 (American Heritage Dictionary of the English Language (4th ed. 2000)) at 476. Under the plain language of the claims, therefore, the boundaries of the JFET region are the edges of the first and second source regions. This is illustrated in Figure 1 below, which is annotated to show the JFET region defined between the first and second source regions as claimed:



'633 Patent, Fig. 1 (annotated).

The specification of the '633 Patent provides a conflicting definition of the JFET region. In the specification, the JFET region is bound by the *p* wells of the MOSFET device, not the source regions. *Id*. at 5:23-26 ("The semiconductor device 10 also includes … a junction field-effect transistor (JFET) region 30 formed between the wells 26, 28."), 6:3-5 ("The remaining region of the additional epitaxial layer between the wells 26, 28 forms the JFET region 30."). This is shown in the annotated version of Figure 1 below, where the JFET region (pink) is defined between the first and second *p* wells (cyan):



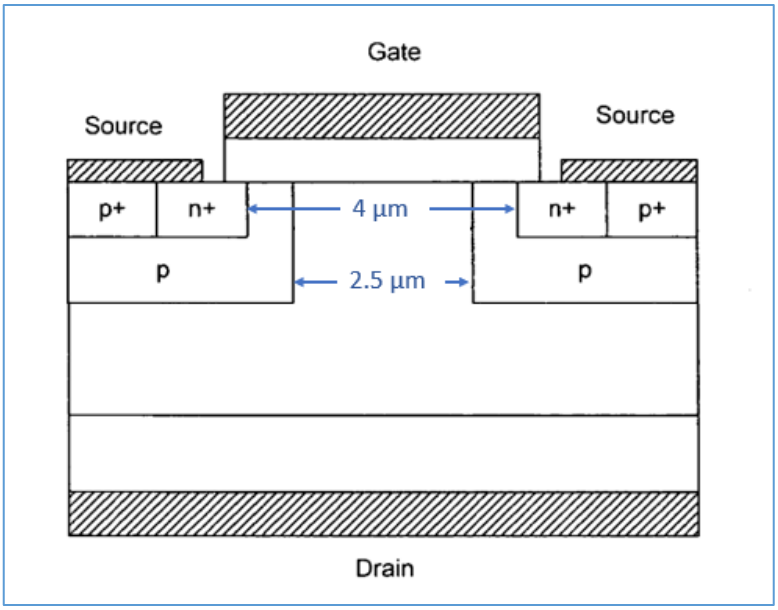
Id., Fig. 1 (annotated).

The specification also identifies element 36 as the "width" of the JFET region 30, and illustrates the width as generally aligned with the edges of the *p* wells 26, 28, rather than the source regions 46, 48. *Id*. at 6:16-27, Fig. 1. The specification further explains that the *p* wells and JFET region are doped with impurities having different polarities. *Id.* at 5:42-45 ("[T]he wells 26, 28 are doped with a P-type impurity to a 'P' concentration whereas the JFET region 30 is doped with N-type impurities to an 'N' concentration.").

Thus, while the plain language of the claims defines the JFET region in a way that includes portions of *p* wells, the specification expressly distinguishes them from one another.

As detailed in the accompanying declaration of Dr. Doolittle, the specification's description of the JFET region is consistent with the understanding of a POSITA. Ex. 1 ¶ 57. Those of skill in the art understood that the JFET region of an *n* channel MOSFET device was typically defined between the *p* wells. *Id*. That understanding—and the description of the JFET region in the specification of the '633 Patent—cannot be reconciled with the plain language of claim 9, which defines the JFET region as the area between the first and second source regions, and thus includes portions of the *p* wells. *Id*.

When there is "an irreconcilable contradiction" between the specification and the claim language, such as here, the claims are indefinite. *Enzo Life Scis., Inc. v. Digene Corp.*, 305 F. Supp. 2d 406, 410 (D. Del. 2004); *see also Allen Eng'g Corp. v. Bartell Indus., Inc.*, 299 F.3d 1336, 1349 (Fed. Cir. 2002) (claims held indefinite where "the specification describes this structure in contrary terms"). The contradiction is particularly meaningful here because the width of a JFET region will vary depending on whether it is measured between the source regions or *p* wells. Ex. 1 ¶ 58. That variability could mean that a given MOSFET devices falls within or outside the scope of the claims depending on where it is measured. *Id*. Dr. Doolittle illustrated this concern in the image below, where the JFET width would fall within the scope of claim 9 ("less than about three micrometers") if measured between the *p* wells, but would fall outside the scope of claim 9 if measured between the source regions:



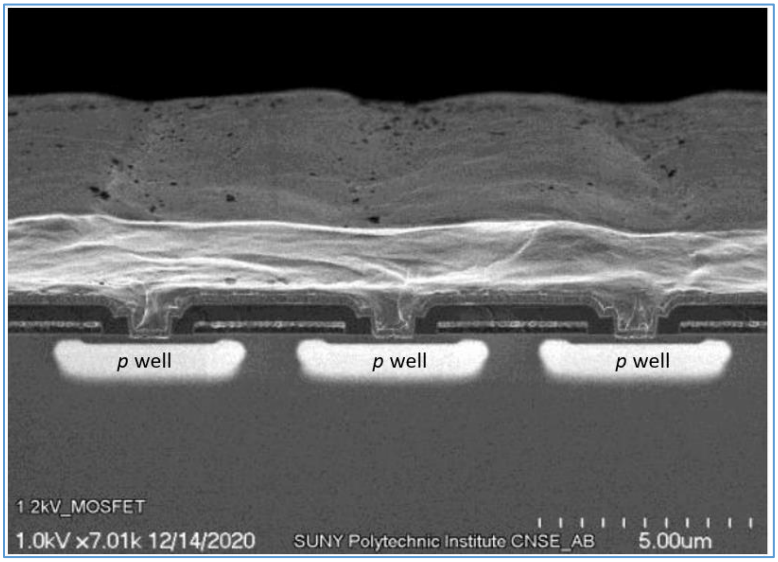
Id.

This is the "zone of uncertainty" the law of indefiniteness is designed to prevent. *Nautilus*, 572 U.S. at 909. When a claim term "is open to multiple interpretations reflecting markedly different understandings of the patent's scope," it fails to provide the reasonable certainty the law requires. *Id*. at 913. And "it is not the courts' function to rewrite claims to preserve their validity." *Allen*, 299 F.3d at 1349 (cleaned up). When the claims conflict with the specification, a finding of indefiniteness is warranted. *Id*.[4]

2. The Claims and Specification Do Not Describe Where Along the Boundary of the JFET Region to Take the Width Measurement

[4] It appears that Purdue will ask the Court to fix the contradiction between the claims and specification by rewriting the term "defined between" to mean "located between." *See* Ex. 2 at 129:13-130:2. Doing so would be contrary to the Federal Circuit's holding in *Allen* and would frustrate the public notice function by effectively changing the scope of the patent claims from when they were originally issued. *See* 299 F.3d at 1349; *Nautilus*, 572 U.S. at 899.

The Asserted Claims are also indefinite because the JFET region will have different width measurements depending on where along its boundary the measurement is taken. *See* Ex. 1 ¶¶ 61-63. To prove infringement in this case, Purdue will have to show that the JFET region in the accused products—which are real-world MOSFET devices—satisfy the width dimensions recited in claims 9 and 10. As Dr. Doolittle explains, the JFET region in a real-world MOSFET has significant curvature along its outer boundaries resulting from the implantation process of the source regions and *p* wells. *Id*. The curvature is illustrated in the example MOSFET depicted below, where the distance between *p* wells varies between the top and bottom of their edges:

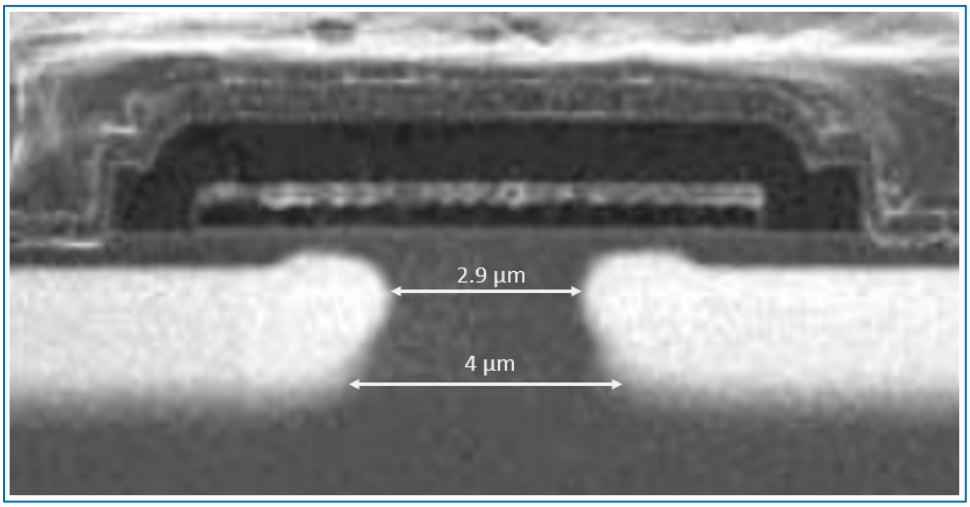


Id. ¶ 62.[5]

Due to the curvature of the *p* well boundaries, the width measurement of the JFET region will vary depending on where it is taken. Dr. Doolittle illustrated this point in the

[5] Dr. Doolittle explained that the same issue would be present if the JFET region is defined between the source regions (as recited in the claim language). *Id*. ¶ 60.

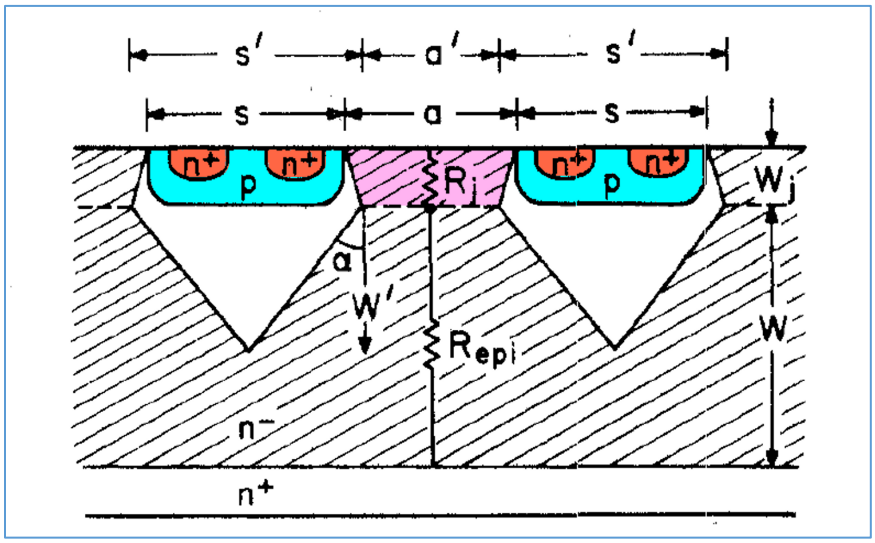
image below. *Id.* ¶ 63. If the JFET width is measured at the upper end of the *p* wells, then it falls within the scope of claim 9 ("a width less than about three micro-meters"). If, however, the JFET width is measured at the lower end of the *p* wells, then it falls outside of the claim requirements:



Id.

The specification of the '633 Patent does not resolve this ambiguity or explain where along the boundary of the JFET region the width measurement should be taken. *Id.* ¶¶ 64-65. Figure 1 of the patent illustrates a JFET region 30 having vertical edges with slight curvature along the lower boundary. *See* '633 Patent, Fig. 1. The specification does not, however, explain whether or how to account for the curvature when taking that measurement. *Id.* at 6:16-62. Figure 1 is also a simplified cartoon drawing of the MOSFET device that is not drawn to scale. *See Hockerson-Halberstadt, Inc. v. Avia Group Int'l, Inc.*, 222 F.3d 951, 956 (Fed. Cir. 2000). Thus, it does not reflect the degree of curvature that would exist in a real-world device. Ex. 1 ¶ 65.

The lack of detail in the specification stands in contrast to the prior art, which recognizes that a JFET region will have varying dimensions depending on where it is measured. In a 1984 research paper titled, *Optimum Design of Power MOSFET's* ("Hu"), the authors illustrated a JFET region (pink) defined between two *p* wells (cyan):



Ex. 6, Fig. 1(b) (annotated).

The paper explains that the narrowest portion of the JFET region is the neck, which is identified in Figure 1(b) as element *a'*. *Id*. at 1693. The wider portion of the JFET region, which is measured directly below the gate oxide and extends between the upper corners of the *p* wells is identified as element *a*. *Id*. Thus, Hu provides two specific locations to measure the width of the JFET region and identifies each location with a unique symbol. *Id*. The '633 Patent fails to provide that level of detail or guidance, leaving a POSITA to arbitrarily decide where along the curved boundary of a given JFET region its width should be measured. Ex. 1 ¶¶ 64-68.

In the wake of *Nautilus*, courts have consistently found claims indefinite where a parameter can be measured using different techniques that produce different results, but

the patent fails to explain which technique should be used. In *Saso Golf, Inc. v. Nike, Inc.*, the Federal Circuit held that a claim reciting "radius of curvature" was indefinite because "there are multiple methods of calculating the radii of curvature because the calculations depend on pinpointing the locations of the toe and heel," and "[n]othing in the record indicates that an artisan would inherently know the locations of those boundaries and the patent provides no guidance." 843 F. App'x 291, 297 (Fed. Cir. 2021). The Federal Circuit reached the same result in *Dow*, where claims required measurement of a molecular weight, the method chosen for calculating the weight could affect whether or not a given product infringed the claims, and the patent failed to specify which method should be used. 803 F.3d at 630. And in *Nichia Corp. v. VIZIO, Inc.*, claims that required a particular phosphor concentration were held indefinite because "there are multiple ways to measure phosphor concentration," the patent failed to identify "a particular way to measure," and "different concentration measurement methods could result in different conclusions about whether a particular concentration is larger or smaller than another." No. 16-cv-545, 2018 WL 11350040, at *17 (C.D. Cal. May 29, 2018).

In the Asserted Claims of the '633 Patent, there are multiple locations along the boundary of the JFET region to measure its width, the patent does not specify where the measurement should be taken, and a given device may fall within or outside the scope of the claims depending on which location is chosen. Ex. 1 ¶ 68. This lack of guidance in the patent disclosure renders the claims indefinite. *Teva*, 789 F.3d at 1341-42; *Dow*, 803 F.3d at 630.

Because the claims and specification of the '633 Patent offer conflicting definitions of the JFET region, and because the patent fails to specify how and where to measure the width of the JFET region, a POSITA would not be able to determine the scope of the claims with reasonable certainty. The claims are thus indefinite. *Nautilus*, 572 U.S. at 910.

C. "the JFET region having a width less than about three micrometers" (claim 9)

Wolfspeed's Proposal	Purdue's Proposal
Indefinite	No construction necessary.

Claim 9 of the '633 Patent requires the JFET region to have a width that falls within the range of "less than about three micrometers." '633 Patent, claim 9. When a claim recites a range of values in this manner, the patent must provide objective guidance to determine both the lower and upper bound of the range with reasonable certainty. *See Amgen, Inc. v. Chugai Pharm. Co., Ltd.*, 927 F.2d 1200, 1217–18 (Fed. Cir. 1991). The '633 Patent fails to provide those objective boundaries.

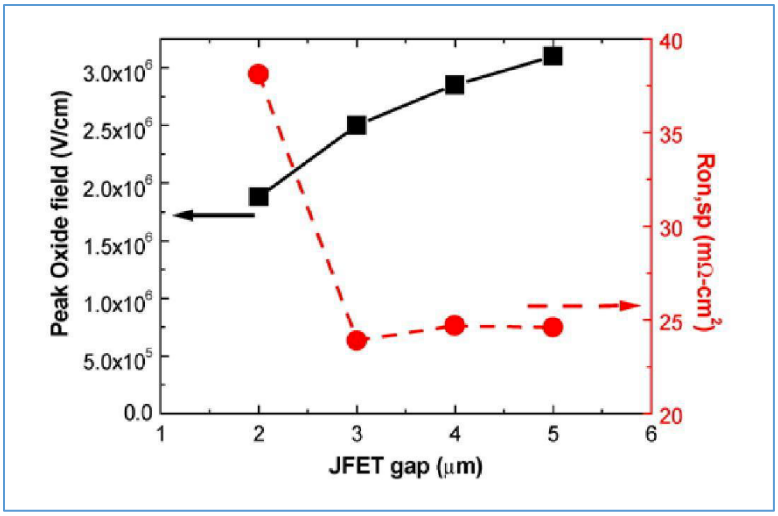
1. The Patent Does Not Specify a Lower Bound for the Claimed Range

The literal language of claim 9 encompasses a range of width values between zero and "about three micrometers." '633 Patent, claim 9; Ex. 1 ¶ 74. With respect to the lower end of the range, the parties and their experts appear to agree that a value of zero falls outside the scope of the claim because a JFET region with zero width would be incapable of passing current and would render the MOSFET device inoperable. *Id.*; Ex. 4 ¶ 46. Because the claims do not cover a width of zero, the question becomes what the minimum allowable width is. Ex. 1 ¶ 74. The '633 Patent fails to answer that question with reasonable

certainty. *Id*. ¶ 75.

The specification does not identify any specific lower bound for the claimed JFET width that would result in an operable device. *Id*. Its descriptions of the JFET width are generic and generally parrot the claim language. *See*, *e.g.*, '633 Patent at 1:65-67 ("The JFET region may have a width less than about three micrometers. For example, the JFET may have a width of about one micrometer."), 2:47-49, 6:24-27. The specification also fails to specify the value of any performance metrics that might dictate a minimum width for the JFET region. Ex. 1 ¶ 76. The patent discusses reduction of on-state resistance and higher blocking voltages as general design goals, but never specifies acceptable values for those parameters that would provide a POSITA with guidance to determine the minimum acceptable JFET region width. *Id*.; '633 Patent at 6:16-7:38.

Once again, the lack of description in the specification stands in contrast to the prior art, which provides a far more detailed analysis of how to determine optimal JFET widths. Ex. 1 ¶ 77. For example, a 2001 paper titled, *Design and Process Issues for Silicon Carbide Power DiMOSFETs* ("Ryu 2001") analyzed the on-state resistance and oxide field strength as a function of JFET width for a 2000-volt SiC MOSFET:



Ex. 7, Fig. 2.

In the depicted graph, the on-state resistance (red) and oxide field strength (black) vary as a function of the JFET width shown along the bottom axis. *Id*. Based on these values, the authors determined a JFET width of 3 microns was optimal for a specific 2000V MOSFET device. This type of analysis might inform a POSITA about the lowest acceptable JFET width for a particular device, but is entirely missing from the '633 Patent. Ex. 1 ¶ 77; '633 Patent at 2:29-58, 6:16-7:38.

It is also important to note that the optimal JFET width for one MOSFET is not necessarily optimal for another. For example, Ryu-2001 determined that a 3-micron gap was optimal for a specific MOSFET with a 2000V operating voltage. Ex. 7 at 7. Devices with different operating voltages and current characteristics will have different acceptable JFET widths. Ex. 1 ¶¶ 77, 79. A higher operating voltage generally requires a wider JFET gap to account for the higher oxide fields that "pinch" current flow through the device. *Id*. On the other hand, low-current devices allow for a narrower JFET region, even at higher voltages, because on-state resistance is less of a design concern—a point Dr. Doolittle

explained in his deposition. Ex. 9 at 83:17-86:18. The '633 Patent does not limit itself to any particular voltage or current characteristics that might help a POSITA determine the minimum acceptable JFET width. *See* '633 Patent at 4:35-67, 6:42-62. Thus, the POSITA would be left to guess which values fall within and outside of the claims. *See* Ex. 1 ¶¶ 76-77.

Because a POSITA would not have reasonable certainty about the lower limit of the claimed range, the phrase "less than about three micrometers" renders claim 9 indefinite. *See Enviro Tech Chem. Servs., Inc. v. Safe Foods Corp.*, No. 4:21-CV-00601-LPR, 2022 WL 17721179, at *13 (E.D. Ark. Dec. 15, 2022) (finding claim reciting range "about 7.6 to about 10" indefinite due to the lack of objective upper or lower boundaries) (citing *Nautilus*, 572 U.S. at 910).

2. The Patent Does Not Specify an Upper Bound for the Claimed Range

The upper end of the range recited in claim 9 of the '633 Patent is defined by the phrase "about three micrometers." In patent claiming, the word "about" is known as a "term of degree." *Cf. Ecolab, Inc. v. Envirochem, Inc.*, 264 F.3d 1358, 1367 (Fed. Cir. 2001); *Synthes (USA) v. Smith & Nephew, Inc.*, 547 F. Supp. 2d 436, 454 (E.D. Pa. 2008). It suggests that some value above or below "three micrometers" bounds the upper limit of the claimed range. Terms of degree do not automatically render a patent claim indefinite. *Interval Licensing*, 766 F.3d at 1370. When a term of degree is employed, however, the specification or prosecution history must provide objective boundaries sufficient to determine its scope. *Id.* at 1370-71. In the absence of objective boundaries, the claim is

indefinite. *Id*.

The specification and prosecution history of the '633 Patent fail to provide objective boundaries for the phrase "about three micrometers." As discussed above, the descriptions of the JFET width in the specification are generic and simply mimic the claim language. *See*, *e.g.*, '633 Patent at 1:65-67 ("The JFET region may have a width less than about three micrometers."), 2:47-49, 6:24-27. The specification does not elaborate on the term "about," or specify the range of values it is intended to encompass. *Id*. The same is true of the prosecution history. Because the prior art of record fell squarely within the claimed range, Purdue never elaborated on the scope of meaning of the term "about," or explain how far from three microns one could stray without falling outside of the claimed range. *See*, *e.g.*, Ex. 3 at 19-20 (October 12, 2007 Final Rejection at 3-4), 49-50 (March 12, 2008 Response at 10-11).

In these circumstances, the term "about" renders claim 9 indefinite. *See Synthes*, 547 F. Supp. 2d at 454. In *Synthes*, the court found the term "less than about 2%" indefinite because "it is impossible to tell exactly what" fell within the scope of the claims. *Id*. The specification and prosecution history failed to provide guidance regarding the scope or tolerance of the claimed percentage. *Id.* Thus, the court explained, "a competitor whose plate has a … ratio of 2.5%, or even 3% or 4%, would not know if he is infringing because there is no indication how much above the 2% threshold the claims at issue actually include." *Id*. The same is true with respect to claim 9 of the '633 Patent. Without objective boundaries or guidance in the specification and prosecution history, a competitor or potential infringer is left to guess whether JFET widths of 3.1, 3.5, or 4 microns are within

the scope of the claim, with no reasonable certainty as to the upper limit. Again, this is the "zone of uncertainty" indefiniteness guards against. *Nautilus*, 572 U.S. at 909; *see also Berkheimer v. HP Inc.*, 881 F.3d 1360, 1364 (Fed. Cir. 2018) (the term "minimal redundancy" is indefinite because the patent fails to explain "how much redundancy is permitted").

Perhaps realizing the lack of guidance in the specification, Purdue relies on expert testimony to fill the gap. In his claim construction declaration, Purdue's expert Dr. Shanfield testifies that the acceptable tolerance should be derived from a "manufacturing tolerance" consisting of "a distribution with range and standard deviation" from "the specified value." Ex. 4 ¶¶ 43-45. In another case involving the '633 Patent, Purdue's expert also suggested that an acceptable range for the term "about" would be ± 10%. *See* Ex. 1 ¶ 83 (citing Declaration of Dr. Ishwara Bhat). That testimony finds no support in the intrinsic record of the '633 Patent. The patent does not discuss "manufacturing tolerances" or provide any reference to understand the scope of permissible tolerances for the JFET region of a SiC MOSFET device. *See*, *e.g.*, '633 Patent at 1:65-67, 2:47-49, 6:25-27. And the selection of a ± 10% tolerance appears to be completely arbitrary.[6]

[6] Dr. Shanfield also cites a 2007 paper from the named inventors to show that the "figure of merit" for a particular MOSFET device does not improve at JFET widths above three microns. Ex. 4 ¶ 47. As an initial matter, the level of analysis contained in the paper is not reflected in the intrinsic record of the '633 Patent. Nor can the paper's analysis be incorporated into the patent or the knowledge of a POSITA because it was published after the filing date of the '633 Patent. *See Nautilus*, 572 U.S. at 899 ("definiteness is to be measured as of the time of the patent application."). Moreover, the paper does not specify which values above three microns would be acceptable. Ex. 1 ¶¶ 83-86.

While a POSITA would understand that manufacturing tolerances are generally expected in context of semiconductor design and manufacturing, the degree of acceptable tolerances would vary from one device to the next depending on design goals. *See* Ex. 1 ¶ 79. There is no universally accepted tolerance such that a POSITA would know how much variation is permitted by the term "about." *Id*. And because the intrinsic record of the '633 Patent fails to provide objective boundaries for making that determination, the term "about three micrometers" renders claim 9 indefinite.

D. "the JFET region has a width of about one micrometer" (claim 10)

Wolfspeed's Proposal	Purdue's Proposal
Indefinite	No construction necessary.

Claim 10 of the '633 Patent depends from claim 9 and further specifies that "the JFET region has a width of about one micrometer." '633 Patent, claim 10. This phrase renders claim 10 indefinite for the reasons discussed above with respect to the phrase "about three micrometers" in claim 9. *See* V.C.2 *supra*. The specification and prosecution history of the '633 Patent do not provide objective boundaries to determine the range of acceptable widths above and below one micron, leaving a competitor to guess as to the scope of the claim. *See Synthes*, 547 F. Supp. 2d at 454.

VI. CONCLUSION

For the above reasons, Wolfspeed respectfully requests that the Court adopt its proposed constructions.

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Respectfully submitted,

/s/ Richard W. Erwine

Richard W. Erwine
Raymond N. Nimrod
QUINN EMANUEL URQUHART & SULLIVAN, LLP
51 Madison Avenue, 22nd Floor
New York, New York 10010
Telephone: (212) 849-7000
Facsimile: (212) 849-7100
raynimrod@quinnemanuel.com
richarderwine@quinnemanuel.com

Jared Newton
QUINN EMANUEL URQUHART & SULLIVAN, LLP
1300 I Street NW
Washington, D.C. 20005
Telephone: (202) 538-8000
Facsimile: (202) 538-8100
jarednewton@quinnemanuel.com

Kevin Jang
QUINN EMANUEL URQUHART & SULLIVAN, LLP
50 California Street, 22nd Floor
San Francisco, California 94111
Telephone: (415) 875-6600
Facsimile: (415) 875-6700
kevinjang@quinnemanuel.com

Peter D. Siddoway
SAGE PATENT GROUP
2301 Sugar Bush Road, Suite 200
Raleigh, NC 27609
Telephone: 984-219-3369
Facsimile: 984-538-0416
Email: psiddoway@sagepat.com

Attorneys for Defendant Wolfspeed, Inc.

CERTIFICATE OF SERVICE

I hereby certify that on the 31st of March 2023, I electronically filed the foregoing document with the Clerk of the Court using the CM/ECF system, which will send notification of such filing to all counsel of record.

/s/ *Peter D. Siddoway*

Peter D. Siddoway

CERTIFICATE OF WORD COUNT

Pursuant to Local Rules 7.3, I hereby certify that this Brief complies with the word limit set forth in Local Rule 7.3(d)(1).

/s/ *Peter D. Siddoway*

Peter D. Siddoway